In the Claims

Claim 1 (currently amended): A system comprising:

a housing;

a circuit board supported in the housing;

a plurality of slot connectors supported on the circuit board;

a first card in one of the slot connectors;

a first circuit component mounted on the first card, the slot connector coupling the first circuit component to a power supply;

a second card in another one of the slot connectors;

a second circuit component mounted on the second card; and

an optical interconnect coupling the first card to the second card, the first circuit component being configured to communicate with the second circuit component via the optical interconnect, the optical interconnect being entirely supported by the first and second cards, whereby the optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded.

Claim 2 (original): A system in accordance with claim 1 wherein the optical interconnect comprises a fiber optic cable.

Claim 3 (previously presented): A system in accordance with claim 1 wherein the optical interconnect comprises an optical connector on the first card configured to convert between electrical signals and optical signals, and wherein the system further includes circuit traces on the first card coupling the optical connector to the first circuit component.

Claim 4 (previously presented): A system in accordance with claim 1 wherein the optical interconnect comprises an optical connector on the second card configured to convert between electrical signals and optical signals, and wherein the system further includes circuit traces on the second card coupling the optical connector to the second circuit component.

Claim 5 (previously presented): A system in accordance with claim 1 wherein the optical interconnect comprises a first optical connector, on the first card, configured to convert between electrical signals and optical signals, wherein the system further includes circuit traces on the first card coupling the first optical connector to the first circuit component, wherein the optical interconnect further comprises an optical connector, on the second card, configured to convert between electrical signals and optical signals, the system further including circuit traces on the second card coupling the second optical connector to the second circuit component.

Claim 6 (original): A system in accordance with claim 1 wherein the second circuit component comprises a DRAM.

Claim 7 (original): A system in accordance with claim 1 wherein the second circuit component comprises a synchronous link type DRAM.

Claims 8-13 (cancelled).

Claim 14 (original): A computer comprising:

a housing;

a circuit board supported in the housing;

a plurality of connectors supported on the circuit board;

a first card in a first one of the connectors;

a processor supported by the first card;

a second card in a second one of the connectors;

a synchronous link DRAM memory supported by the second card;

a power supply in the housing;

conductors coupling the power supply to the processor via the first connector, the conductors including circuit traces on the first card;

conductors coupling the power supply to the memory via the second connector, the conductors including circuit traces on the second card; and

an optical interconnect coupling the processor to the memory for data communications, the optical interconnect being within the housing, in use, wherein the optical interconnect does not pass through the connectors.

Claim 15 (original): A computer in accordance with claim 14 and further comprising a third card in a third one of the connectors, a co-processor supported by the third card, and an optical interconnect coupling the co-processor to the processor.

Claim 16 (original): A computer in accordance with claim 15 and further comprising conductors coupling the power supply to the co-processor via the third connector, the conductors including circuit traces on the third card.

Claim 17 (original): A computer in accordance with claim 15 wherein the co-processor is a math co-processor.

Claim 18 (original): A computer in accordance with claim 15 and further including an electronic device in the housing capable of generating electromagnetic interference, and wherein the optical interconnect shields communications between the processor and the memory from the electromagnetic interference.

Claim 19 (original): A computer comprising:

a housing;

a circuit board supported in the housing;

a plurality of connectors supported on the circuit board;

a first card in a first one of the connectors;

a first integrated circuit supported by the first card;

a second card in a second one of the connectors;

a second integrated circuit supported by the second card;

a power supply in the housing;

conductors coupling the power supply to the first integrated circuit via the first connector, the conductors including circuit traces on the first card;

conductors coupling the power supply to the second integrated circuit via the second connector, the conductors including circuit traces on the second card; and

an optical interconnect coupling the first integrated circuit to the second integrated circuit for data communications, the optical interconnect being within the housing, in use, wherein the optical interconnect does not pass through the connectors.

Claim 20 (original): A computer in accordance with claim 19, and further comprising a third card in a third one of the connectors, a co-processor supported by the third card, and an optical interconnect coupling the co-processor to the processor wherein the first integrated circuit comprises a processor, and wherein the second integrated circuit comprises a memory.

Claim 21 (original): A computer in accordance with claim 20 and further comprising conductors coupling the power supply to the co-processor via the third connector, the conductors including circuit traces on the third card.

Claim 22 (original): A computer in accordance with claim 20 wherein the co-processor is a math co-processor.

Claim 23 (original): A computer in accordance with claim 20 and further including an electronic device in the housing capable of generating electromagnetic interference, and wherein the optical interconnect shields communications between the processor and the memory from the electromagnetic interference.

Claim 24 (previously presented): A method of assembling a system, the method comprising:

supporting a circuit board in a housing;

supporting a plurality of slot connectors on the circuit board;

mounting a first circuit component on a first card;

inserting the first card into a first one of the slot connectors;

mounting a second circuit component on a second card;

inserting the second card into a second one of the slot connectors; and

flexibly optically coupling the first card to the second card for optical communications between the first circuit component and the second circuit component, using a first optical connector supported by the first card and completely movable with the first card, a second

optical connector supported by the second card and completely movable with the second card, and an optical cable coupled between the first and second optical connectors, whereby the flexible optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded.

Claim 25 (original): A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises using a fiber optic cable.

Claim 26 (original): A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises supporting an optical connector on the first card to convert between electrical signals and optical signals, and forming circuit traces on the first card to couple the optical connector to the first circuit component.

Claim 27 (original): A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises supporting an optical connector on the second card to convert between electrical signals and optical signals, and forming circuit traces on the second card to couple the optical connector to the second circuit component.

Claim 28 (original): A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises supporting an optical connector on the first card to convert between electrical signals and optical signals, forming circuit traces on the first card to couple the optical connector to the first circuit component, supporting an optical connector on the second card to convert between electrical signals and optical signals, and forming circuit traces on the second card to couple the optical connector to the second circuit component.

Claim 29 (original): A method of assembling a system in accordance with claim 24 wherein mounting the second circuit component comprises mounting a DRAM on the first card.

Claim 30 (original): A method of assembling a system in accordance with claim 24 wherein mounting the second circuit component comprises mounting a synchronous link type DRAM on the first card.

Claim 31 (original): A method comprising:

supporting a circuit board in a housing;

supporting a plurality of slot connectors on the circuit board;

supporting a processor on a first card having an edge connector;

inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board;

providing a second card having an edge connector configured for sliding receipt in a second one of the slot connectors;

supporting a synchronous link DRAM memory on a second card having an edge connector;

inserting the edge connector of the second card into a second one of the slot connectors to support the second card from the circuit board;

supporting a power supply in the housing;

coupling the power supply to the processor via the first slot connector, the coupling including using circuit traces on the first card extending from the edge connector of the first card toward the processor;

coupling the power supply to the memory via the second slot connector, the coupling including using circuit traces on the second card extending from the edge connector of the second card toward the memory; and

optically coupling the processor to the memory for data communications using an optical interconnect within the housing, wherein the optical interconnect does not pass through the slot connectors.

Claim 32 (original): A method in accordance with claim 31 and further comprising supporting a co-processor on a third card having an edge connector, and optically coupling the co-processor to the processor.

Claim 33 (original): A method in accordance with claim 32 and further comprising coupling the power supply to the co-processor via the third slot connector, the coupling comprising using circuit traces on the third card extending from the edge connector of the third card toward the co-processor.

Claim 34 (original): A method in accordance with claim 32 wherein supporting a co-processor comprises supporting a math co-processor on the third card.

Claim 35 (original): A method comprising:

supporting a circuit board in a housing;

supporting a plurality of slot connectors on the circuit board;

supporting a first integrated circuit on a first card having an edge connector;

inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board;

providing a second card having an edge connector configured for sliding receipt in a second one of the slot connectors;

supporting a second integrated circuit on a second card having an edge connector;

inserting the edge connector of the second card into a second one of the slot connectors to support the second card from the circuit board;

supporting a power supply in the housing;

coupling the power supply to the first integrated circuit via the first slot connector, the coupling including using circuit traces on the first card extending from the edge connector of the first card toward the first integrated circuit;

coupling the power supply to the second integrated circuit via the second slot connector, the coupling including using circuit traces on the second card extending from the edge connector of the second card toward the second integrated circuit; and

optically coupling the first integrated circuit to the second integrated circuit for data communications using an optical interconnect within the housing, wherein the optical interconnect does not pass through the slot connectors.

Claim 36 (original): A method in accordance with claim 35 and further comprising supporting a co-processor on a third card having an edge connector, and optically coupling the co-processor to the processor, wherein the first integrated circuit comprises a processor, and wherein the second integrated circuit comprises a memory.

Claim 37 (original): A method in accordance with claim 36 and further comprising coupling the power supply to the co-processor via the third slot connector, the coupling comprising using circuit traces on the third card extending from the edge connector of the third card toward the co-processor.

Claim 38 (original): A method in accordance with claim 36 wherein supporting a co-processor comprises supporting a math co-processor on the third card.

Claims 39-40 (cancelled).